Digital Adjustment of DC-DC Converter Output Voltage in Portable Applications

There are many portable applications that optimize circuit performance by adjusting the output voltage of a DC-DC converter. For instance, many microprocessors can operate at a low voltage to save power, and then operate at a high voltage for increased processing power. Switching between these operating modes requires adjusting the output voltage of a DC-DC converter. Another example is an LCD display; as its temperature changes, the voltage applied to it must change to maintain the correct contrast ratio.

Adjustments made via digital control have proven to be the most reliable method of performing these and other voltage adjustments. A manual trim pot may be used, but it is often large and can suffer from reliability problems due to wear associated with the manual adjustments; furthermore, it cannot be adjusted under microprocessor control. This article discusses several methods of digitally adjusting the output voltage of a DC-DC converter, with emphasis on devices for portable applications.

Different Digital Method

There are three main methods of digitally adjusting the output voltage of a DC-DC converter:

- A digital-to-analog converter (DAC)
- A trim pot (digital potentiometer)
- A PWM output of a microprocessor (MPU)

DACs

A DAC is simply a digitally-controlled voltage source. The digital interface to a DAC can be either serial or parallel. For applications where the DAC update rate is fairly low (such as DC-DC voltage adjustments), serial interfaces are typically used. They are smaller, using only 2 or 3 wires for a serial interface, compared to 8 to 16 wires for a parallel interface. Fewer pins produce smaller packages, and therefore lowers cost.

The main specifications to consider for a DAC are:

- **Supply voltage**: 3V or 5V supplies are typically required for portable applications.
- **Supply current**: low current extends battery life.
- **Output voltage swing**: the output swing is usually from 0V to V_{REF} (the DAC's reference voltage).
- **Number of bits of resolution**: The number of bits of resolution determines how many

adjustment steps the DAC will have. The number of steps is equal to 2^N, where "N" is the number of bits of resolution of the DAC. A 6-bit DAC, for example, will have 2^6, or 64 steps; while an 8-bit DAC will have 2^8, or 256 adjustment steps.

Note: The step size at the DAC output is the output voltage swing divided by the number of DAC steps. For example, the MAX5361, a 6-bit DAC with a 4V output voltage swing, has a step size of 62.5mV (4V output voltage swing / 2^6 steps).

- **Error Sources**: There are several error sources to consider:
  - **Full-Scale Voltage Error**: For DACs with <= 8-bits of resolution, this error is generally the largest, and will have the greatest effect on overall system accuracy. Low-cost devices can have errors as large as ±25%. However, this initial error can be calibrated out. Calibration usually occurs at production test or the error can be compensated for by using an in-system ADC.
  - **Offset Voltage Error**: This can also be a large error source, and can be calibrated out if too large.
  - **Differential Non Linearity (DNL)**: It is usually necessary that the output of the DAC be monotonic (i.e., increasing or flat output change for increasing input code). This requires a DNL of ±1LSB (max).
  - **Integral Non-Linearity (INL)**: This specification is usually tight enough so as to not be important in these applications.
  - **Temperature Coefficient**: The output voltage has a temperature dependence. This error source cannot be calibrated out at production, unless the system is tested over temperature, although it can be calibrated out using an on-board ADC if its temperature drift is low enough. Typically, the temperature drift is small enough so as to not be a problem.
- **Internal or External Voltage Reference**: Inexpensive devices with internal references are available. However, if an accurate system reference (i.e., an external reference) is available, it may be used for improved performance.
- **Type of interface**: serial or parallel. Serial interfaces are required for small size. Typical choices are SPI, I^2C, SMBus, or bit-banging. Bit-banging entails using general purpose I/O pins to provide the controls necessary for the DAC. The type of interface chosen is a function of the interface(s) supported by the system processor.
- **Package size**: smaller is better. Very small SOT or SC70 packages are available.
- **Volatile or Non-Volatile Settings**: Most DACs have volatile output voltage settings (i.e., they forget their output setting if power is removed). This generally does not pose a problem, since most systems have some sort of non-volatile memory, which can be used in conjunction with the DAC. Non-volatile DACs are also available. These devices retain the DAC register setting in on-chip memory so the DAC can "remember" its output setting even if power is removed.

Table 1. Key Specifications for Representative DACs

Specification / Device	MAX5360	MAX5361	MAX5363	MAX5364	MAX5380	MAX5381	MAX5383	MAX5384
Supply Voltage (V)	2.7 to 3.6	4.5 to 5.5	2.7 to 3.6	4.5 to 5.5	2.7 to 3.6	4.5 to 5.5	2.7 to 3.6	4.5 to 5.5

Supply Current (μA Typ)	150	150	150	150	150	150	150	150
Shutdown Current (μA Max)	1	1	1	1	1	1	1	1
Output Voltage Swing	0V to V_{REF}	0V to V_{REF}	0V to V_{REF}	0V to V_{REF}	0V to V_{REF}	0V to V_{REF}	0V to V_{REF}	0V to V_{REF}
Bits of Resolution	6	6	6	6	8	8	8	8
Full Scale Voltage Error (Max)	10%	10%	10%	10%	10%	10%	10%	10%
Full Scale Error Temperature Coefficient (ppm/° C Max)	±40	±40	±40	±40	±40	±40	±40	±40
Offset Voltage Error (mV Max)	±2	±2	±2	±2	±25	±25	±25	±25
Offset Error Temperature Coefficient (ppm/° C Typ)	3	3	3	3	3	3	3	3
DNL (Max LSBs)	±1	±1	±1	±1	±1	±1	±1	±1
INL (Max LSBs)	±1	±1	±1	±1	±1	±1	±1	±1
Reference Type	2V, Internal	4V, Internal	2V, Internal	4V, Internal	2V, Internal	4V, Internal	2V, Internal	4V, Internal
Interface Type	Serial, I^2C	Serial, I^2C	Serial, SPI	Serial, SPI	Serial, I^2C	Serial, I^2C	Serial, SPI	Serial, SPI
Package Size (SOT23)	5-Pin	5-Pin	6-Pin	6-Pin	5-Pin	5-Pin	6-Pin	6-Pin
Volatile / Non-Volatile	Volatile	Volatile	Volatile	Volatile	Volatile	Volatile	Volatile	Volatile
Power-Up State	Zero Scale	Zero Scale	Zero Scale	Zero Scale	Zero Scale	Zero Scale	Zero Scale	Zero Scale

Design Example (Adjustable LCD Output Voltage)

In the circuit of Figure 1, assume that it is desired to have the DC-DC converter's V_{OUT} to be adjustable from a low of $V_{OUT(MIN)}$ to a high of $V_{OUT(MAX)}$.
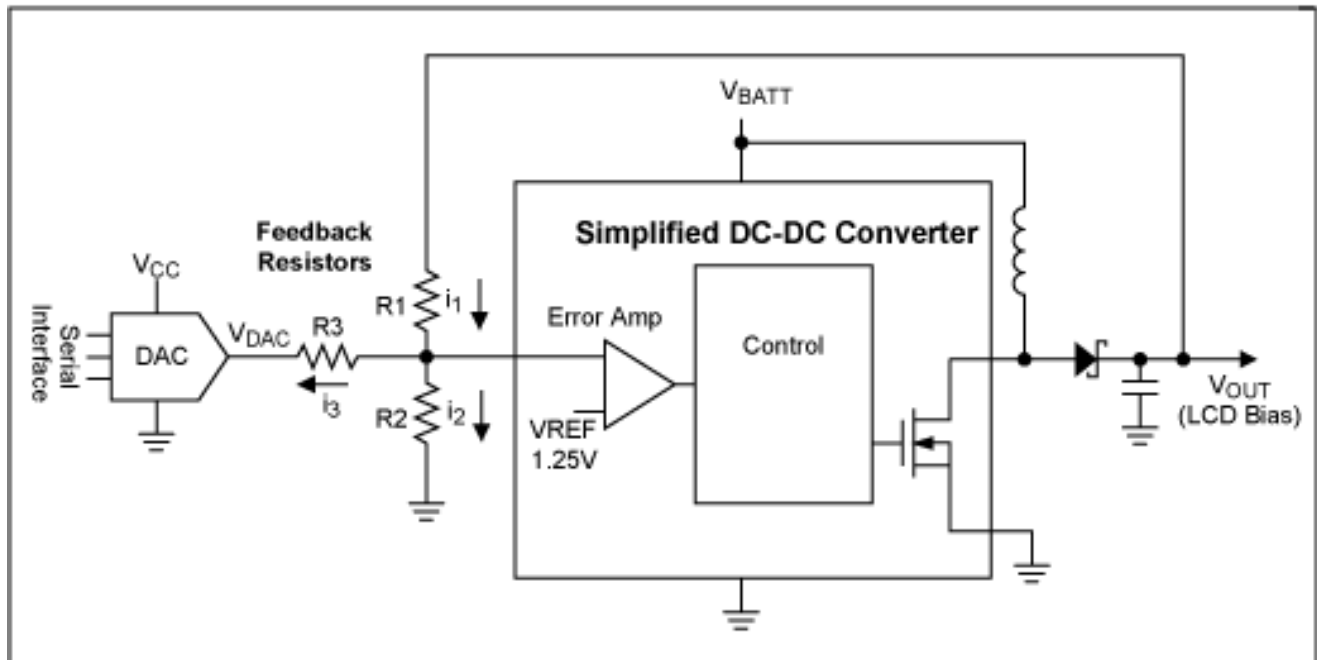

Figure 1. DC-DC converter with DAC for V_{OUT} adjustment.

The highest DAC output voltage is $VDAC_{HIGH}$. Due to the error sources listed above, there is a tolerance on the $VDAC_{HIGH}$ voltage. The higher voltage is $VDAC_{HIGH(MAX)}$, and the lower voltage is $VDAC_{HIGH(MIN)}$. Similarly, the low output voltage has a low and high voltage limit, $VDAC_{LOW(MAX)}$ and a $VDAC_{LOW(MIN)}$, respectively.

R1, R2, R3, and the reference all have errors, resulting in the following MIN and MAX variables for these parameters : $R1_{MAX}$, $R1_{MIN}$, $R2_{MAX}$, $R2_{MIN}$, $R3_{MAX}$, $R3_{MIN}$, $V_{REF(MAX)}$, $V_{REF(MIN)}$.

The output voltage of the LCD (V_{OUT}) can be calculated by noting the following:

1. $V_{OUT} = V_{REF} + i_1 R1$
2. $i_1 = i_2 + i_3$
3. $i_2 = V_{REF}/R2$
4. $i_3 = (V_{REF} - V_{DAC}) / R3$

Substituting equations 2 Ð 4 into equation 1 yields:

5. $V_{OUT} = V_{REF}(1 + (R1/R2)) + (V_{REF} - V_{DAC}) (R1/R3)$

From equation 5, it can be seen that the maximum output voltage occurs for the minimum DAC voltage, and that the minimum output voltage occurs for the maximum DAC voltage.

To ensure that the desired output swing is achieved, choose values of R1, R2, and R3 such that equations 6 and 7 are met:

6. $V_{OUTMAX(LOW)} = V_{REFMIN}(1 + (R1_{MIN}/R2_{MAX})) + (V_{REFMIN} - V_{DACMIN(HIGH)})(R1_{MIN}/R3_{MAX})$

7. $V_{OUTMIN(HIGH)} = V_{REFMAX}(1 + (R1_{MAX}/R2_{MIN})) + (V_{REFMAX} - V_{DACMAX(LOW)})(R1_{MAX}/R3_{MIN})$

Equation 6 refers to $V_{OUTMAX(LOW)}$, instead of just V_{OUTMAX}. Since there are tolerances on the variables on the right hand side of equation 6, the maximum output voltage also has a tolerance, and can vary from a minimum of $V_{OUTMAX(LOW)}$ to a maximum of $V_{OUTMAX(HIGH)}$. To ensure that the output swings high enough under all possible conditions, equation 6 refers to the lowest possible voltage of V_{OUTMAX}, namely $V_{OUTMAX(LOW)}$.

Similarly, in equation 7, the variables all have tolerances, so V_{OUTMIN} can vary from a minimum of $V_{OUTMIN(LOW)}$ to a maximum of $V_{OUTMIN(HIGH)}$. To ensure that the output swings low enough under all possible conditions, equation 7 refers to the highest possible voltage of V_{OUTMIN}, namely $V_{OUTMIN(HIGH)}$. Note that in equations 6 and 7, V_{OUTMAX} and V_{OUTMIN} are known values, where V_{OUTMAX} is the maximum desired LCD output voltage, and V_{OUTMIN} is the minimum desired output voltage. The minimum and maximum DAC output voltages (V_{DACMIN} and V_{DACMAX}) can be found in the electrical characteristics table of the DAC being used.

The unknown values are R1, R2, and R3. Since there are three unknowns and only 2 equations, there is more than one unique solution for the values of R1, R2, and R3. The most straightforward way to select values for R1-R3 is to use a spreadsheet and plug in values for the resistors until equations 6 and 7 are met. Resistor values should be large enough to prevent excessive power dissipation. A good beginning point is to choose a value for R2 that has been suggested by the manufacturer of the DC-DC converter. Typically, V_{OUTMAX} will be higher than $V_{OUTMAX(LOW)}$, since the latter is calculated using worst-case values. Using the other extreme worst-case values (substituting MIN for MAX, and MAX for MIN, and LOW for HIGH on the right-hand-side of equation 6) results in the other extreme for V_{OUTMAX} - $V_{OUTMAX(HIGH)}$:

8. $V_{OUTMAX(HIGH)} = V_{REFMAX}(1 + (R1_{MAX}/R2_{MIN})) + (V_{REFMAX} - V_{DACMIN(LOW)})(R1_{MAX}/R3_{MIN})$

(Note: in going from equation 6 to equation 8, $V_{DACMIN(HIGH)}$ was changed to $V_{DACMIN(LOW)}$, without changing the "MIN" term to a "MAX" term. This substitution was not made, since equations 6 and 8 both refer to V_{OUTMAX}, which comes from V_{DACMIN}.)

If $V_{OUTMAX(HIGH)}$ exceeds the maximum voltage rating of the LCD display, the DAC codes which cause the output voltage to exceed the LCD voltage limit must be avoided. For methods on avoiding these codes, see "Compensating for Errors in Digital Adjustment Circuitry" below.

Typically, V_{OUTMIN} will be lower than $V_{OUTMIN(HIGH)}$, since the latter is calculated using worst-case values. Using the other extreme worst-case values (i.e., substituting MIN for MAX, and MAX for MIN, and HIGH for LOW on the right-hand-side of equation 7) results in the other extreme for V_{OUTMIN}, namely $V_{OUTMIN(LOW)}$:

9. $V_{OUTMIN(LOW)} = V_{REFMIN}(1 + (R1_{MIN}/R2_{MAX})) + (V_{REFMIN} - V_{DACMAX(HIGH)})(R1_{MIN}/R3_{MAX})$

(Note: in going from equation 7 to equation 9, $V_{DACMAX(HIGH)}$ was changed to $V_{DACMAX(LOW)}$, without changing the "MAX" term to a "MIN" term. This substitution was not made, since equations 7 and 9 both refer to V_{OUTMIN}, which comes from V_{DACMAX}.)

If $V_{OUTMIN(LOW)}$ is too low for desired operation, the DAC codes which cause the output voltage to go too low must be avoided. For methods on avoiding these codes, see "Compensating for Errors in Digital Adjustment Circuitry" below.

TRIM POT

A digital potentiometer is a digitally adjustable resistor. It is generally placed in the feedback loop of a DC-DC converter, and as its value changes, the converter's output voltage changes.
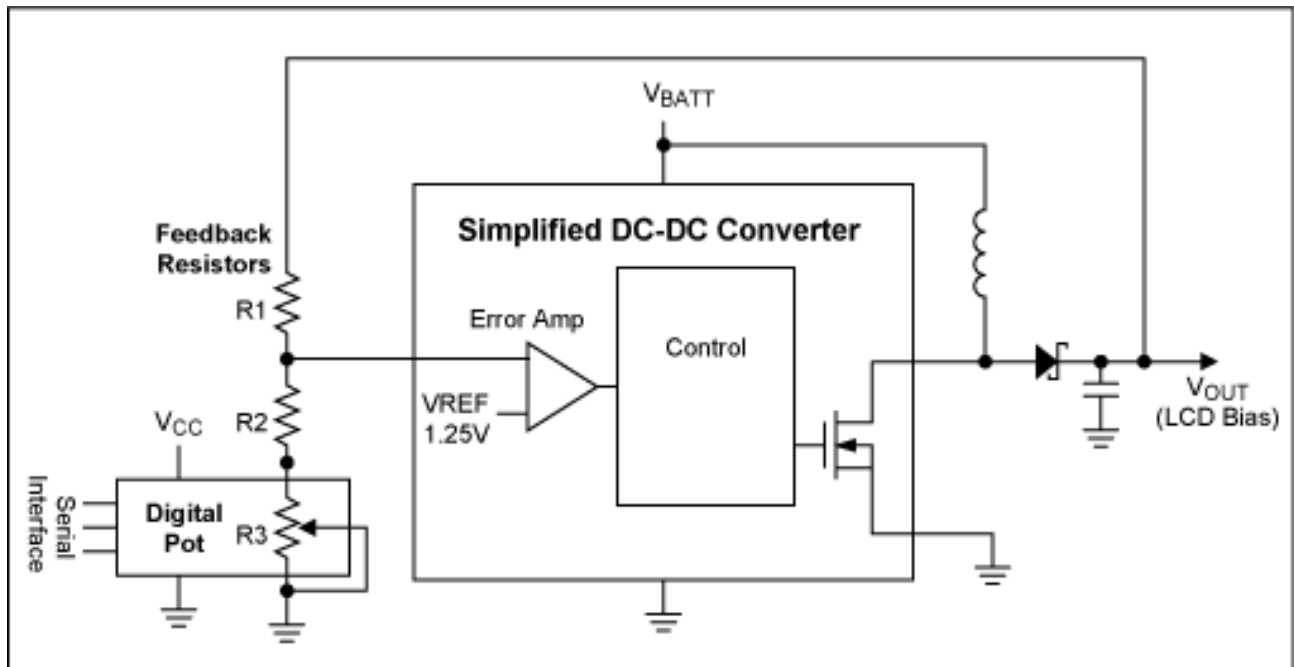

Figure 2. DC-DC converter with digital potentiometer for V_{OUT} adjustment.

In addition to the important specifications listed for a DAC (supply voltage, supply current, DNL, INL, interface type, package size, volatile/non-volatile settings), a trim pot adds the following key specifications:

- **End-to-End Resistance**: The potentiometer resistance typically varies from 0Ω to a maximum value given by the "end-to-end resistance" specification in the product data sheet. There is usually a large tolerance for this value (see "Compensating for Errors in Digital Adjustment Circuitry" below)
- **Wiper Resistance**: This ultimately determines the lowest resistance value of the potentiometer.
- **Operating Voltage Range**: The voltage applied to the high-end, low-end, and wiper of the trim pot must never exceed the operating voltage range of the trim pot
- **Number of steps**: The steps on a digital potentiometer are typically either linear or logarithmic. For LCD adjustment, a linear adjustment is desired. Dividing the end-to-end resistance by the number of steps determines the step size. For example, the MAX5161NEZT is a 32-step digital potentiometer with 200kΩ end-to-end resistance. Dividing 200kΩ by 32 steps, yields 6.25kΩ per step.
- **Error Sources**:
  - **End-to-End Resistance Initial Accuracy:** This error source is generally the largest, and will have the greatest effect on overall system accuracy. Digital potentiometers can have initial errors as large as ±25%. This initial error must be calibrated out. Calibration usually happens at production test, or an in-system ADC can compensate for it, if one is available. See Figures 4 and 5 and "Compensating for Errors in Digital Adjustment Circuitry" below.
  - **Wiper Resistance Initial Accuracy**: This is usually specified very loosely, since the wiper resistance is usually less than the size of one step. This error source can be compensated for using the methods in "Compensating for Errors in Digital Adjustment Circuitry" below.
  - **Temperature Drift of End-to-End Resistance**: The end-to-end resistance has a temperature dependence. This error source is usually not calibrated out at production, unless the system is tested over temperature. However, if the system ADC is stable enough over temperature, it can be used to compensate for temperature errors. Although, the temperature drift is usually small enough so as to not be a problem.

Table 2. Key Specifications for Representative Trim Pots

Specification / Device	MAX5160	MAX5161	MAX5400	MAX5401	MAX5460	MAX5463	MAX5466
Supply Voltage (V)	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5
Operating Voltage (V)	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5
Supply Current (µA Typ)	0.135	0.135	0.1	0.1	0.07	0.07	0.07
End-to-End Resistance (kΩ)	3 Versions: N: 200 M: 100 L: 50	3 Versions: N: 200 M: 100 L: 50	50	100	100	50	10

Wiper Resistance (Ω Typ/Max)	40/1700	400/1700	250/800	250/800	600/1200	600/1200	160/240
Number of Steps	32	32	256	256	32	32	32
End-to-End Resistance Initial Accuracy (Max)	±25%	±25%	±25%	±25%	±25%	±25%	±25%
Temperature Drift of End-to-End Resistance(ppm/° C Typ)	50	50	50	50	35	35	35
DNL (Max LSB)	±1	±1	±1/2	±1/2	±1	±1	±1
INL (Max LSB)	±1/2	±1/2	±1/2	±1/2	±1	±1	±1
Interface Type	Serial: Up / Down	Serial: Up / Down	Serial, SPI	Serial, SPI	Serial: Up / Down	Serial: Up / Down	Serial: Up / Down
Package Size	6-Pin SOT23, 8-Pin µMAX	6-Pin SOT23, 8-Pin µMAX	8-Pin SOT23	8-Pin SOT23	5-Pin SC70, 5-Pin SOT23	5-Pin SC70, 5-Pin SOT23	5-Pin SC70, 5-Pin SOT23
Volatile/Non-Volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile
Power-Up State	Mid-Scale	Mid-Scale	Mid-Scale	Mid-Scale	Mid-Scale	Mid-Scale	Mid-Scale

Design Example

Referring to Figure 2, and using similar naming conventions as in the DAC example, it can be seen by inspection that:

10. $V_{OUT} = V_{REF} \cdot (1 + R1/(R2+R3))$

Note that R3 is the digital potentiometer, and that its value can be changed from $R3_{HIGH}$ to $R3_{LOW}$. Like the DAC, there are MIN and MAX values for these terms. This results in $R3_{HIGH(MIN)}$ and $R3_{HIGH(MAX)}$, as well as $R3_{LOW(MIN)}$ and $R3_{LOW(MAX)}$. These values can be obtained from the data sheet of the digital potentiometer selected.

Similar values as seen in Equations 6-9 can calculated (see Equations 11-14 below) using the same methodology described above. Certain codes can be avoided by using the methods shown below in "Compensating for Errors in Digital Adjustment Circuitry".

11. $V_{OUTMAX(LOW)} = V_{REFMIN} \cdot (1 + R1_{MIN}/(R2_{MAX} + R3_{LOW(MAX)}))$

12. $V_{OUTMIN(HIGH)} = V_{REFMAX} \cdot (1 + R1_{MAX}/(R2_{MIN} + R3_{HIGH(MIN)}))$

13. $V_{OUTMAX(HIGH)} = V_{REFMAX} \cdot (1 + R1_{MAX}/(R2_{MIN} + R3_{LOW(MIN)}))$

14. $V_{OUTMIN(LOW)} = V_{REFMIN} \cdot (1 + R1_{MIN}/(R2_{MAX} + R3_{HIGH(MAX)}))$

PWM Output

Many microprocessors have PWM outputs. These are digital outputs where the duty cycle of the output is adjusted to change the average output voltage. A "DC" voltage is obtained by placing a low-pass output filter at the PWM output. The duty cycle of a PWM output is the percentage of time the output stays high vs. the period of the PWM output. Many microprocessors allow the selection of both the PWM frequency and the PWM duty cycle. For example, the MC68VZ328 microprocessor provides both a 16-bit and an 8-bit PWM output. The number of bits determines the number of adjustment steps of the PWM output. 8-bits is more than adequate for DC-DC converter voltage adjustment, providing 256 steps of PWM adjustment, from 0% duty cycle to 100% duty cycle.
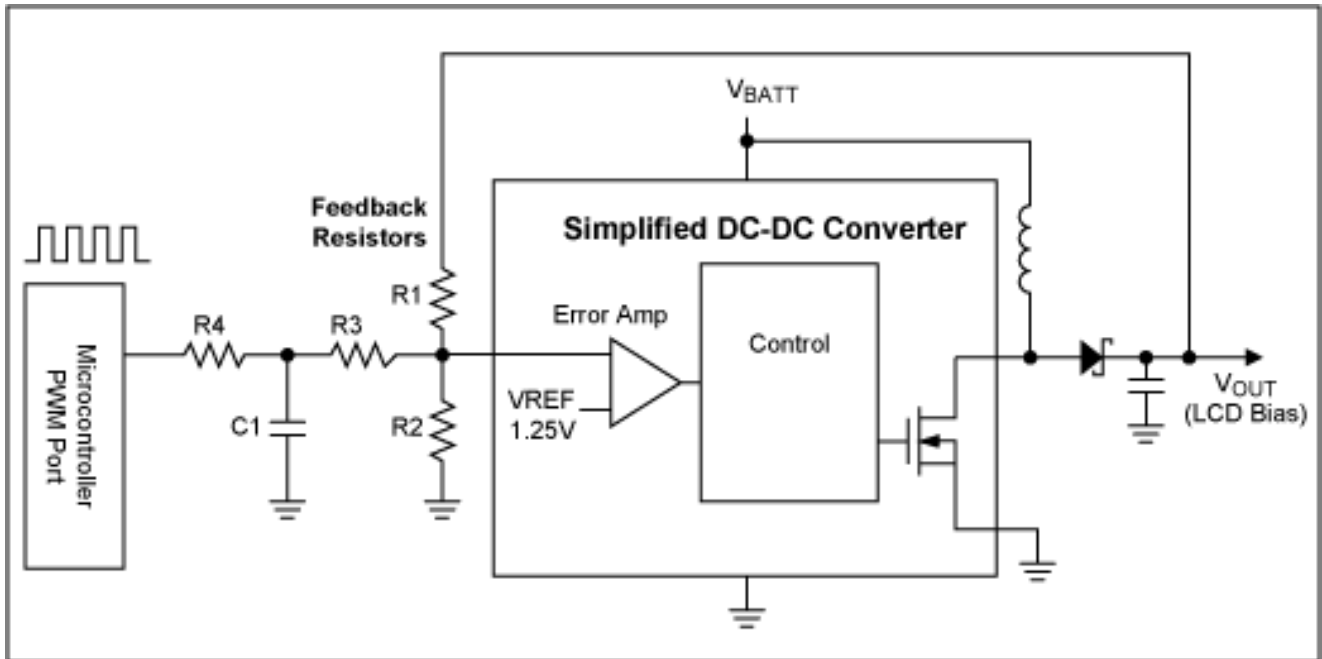

Figure 3. DC-DC converter with PWM for VOUT adjustment.

PWM outputs provide the cheapest method of voltage adjustment, since most microprocessors have at least one PWM output. While inexpensive (since they come with the microprocessor), PWM outputs are costly in terms of power consumption, since they generate a "DC" level by providing a high-frequency output which is subsequently filtered. The high-frequency switching of the PWM output stage consumes much more power than a low-power DAC or digital trim pot, both of which are DC by nature. In Figure 3, filtering of the PWM AC waveform is provided by the R4-C1 combination. R3 is used to isolate C1 from affecting the AC performance of the R1-R2 feedback loop.

PWM outputs are by nature inaccurate, since their output voltages are a function of the digital levels V_{OH} and V_{OL}. Because V_{OH} and V_{OL} are digital output voltage specifications, they are specified very loosely (V_{OH} can be anywhere between V_{OH} min and V_{CC}, the I/O supply to the microprocessor; and

V_{OL} can be anywhere between V_{OL} max and GND). And, since these digital levels are typically a function of V_{CC}, they vary as the supply voltage to the processor varies.

The important specifications for a PWM output are:

- **V_{OH} and V_{OL}**: The specified levels (or ranges) for each, along with the duty cycle determine the nominal (DC) output voltage of the PWM output.
- **Duty Cycle**: both range and accuracy are important. The duty cycle determines what percentage of the time the output will be at V_{OH}, and what percentage it will be at V_{OL}.
- **PWM Frequency:** The frequency is important, since to be useful, the PWM output must be filtered by a low-pass filter. The PWM frequency is used to calculate the attenuation of the PWM ripple (the PWM output swings from V_{OH} to V_{OL}, and to be useful for adjusting a DC-DC converter output, this AC square-wave must be converted to a low-ripple "DC" signal).

Since V_{OL} and V_{OH} are specified so loosely, PWM outputs are really best used in closed-loop systems such as LCD control or audio volume control, where the absolute accuracy isn't important. In these cases, the user simply increases or decreases the voltage as necessary. However, with the inaccuracies posed by the PWM outputs, some measurement must be made to ensure that the PWM signal never causes a high enough output voltage to cause damage to other circuitry. This measurement can be done at production test, by measuring the output voltage of the PWM over certain parameters (temperature, loading of the power supply, etc.). Alternatively, it can be accomplished by measuring the LCD output voltage with an ADC, and keeping the LCD voltage within range via software (see "Compensating for Errors in Digital Adjustment Circuitry" below).

Design Example

Referring to Figures 3 and 1, and using the similar naming conventions as in the DAC example, the output voltage (V_{OUT}) can be calculated by making the following substitutions into equation 5: substitute R3 + R4 for R3; and substitute $V_{PWM} = D \cdot V_{OH} + (1-D) \cdot V_{OL}$ for V_{DAC}. V_{PWM} is the average output voltage of the PWM, D is the duty cycle of the PWM (in %), V_{OH} is the output voltage high voltage, and V_{OL} is the output low voltage.

15. $V_{OUT} = V_{REF}(1 + (R1/R2)) + (V_{REF} - D \cdot V_{OH} + (1-D) \cdot V_{OL})(R1/ (R3 + R4))$

Note that the value of D can be changed from D_{HIGH} to D_{LOW} (typically 100% to 0%, in discrete increments). The duty cycle has tolerance (although it is typically not specified in the processor data sheet), which leads to $D_{HIGH(MAX)}$, $D_{HIGH(MIN)}$, $D_{LOW(MAX)}$, and $D_{LOW(MIN)}$. The digital output voltages V_{OH} and V_{OL} also have tolerances, which lead to $V_{OH(MIN)}$, $V_{OH(MAX)}$, $V_{OL(MIN)}$, and $V_{OL(MAX)}$.

The same values as in equations 6-9 can be calculated (see equations 16-19 below). The duty cycle values which would cause the output voltage to exceed the maximum desired voltage (similar to the digital codes for a DAC or trim pot) can be avoided using the methods shown below in "Compensating for Errors in Digital Adjustment Circuitry".

16. $V_{OUTMAX(LOW)} = V_{REFMIN}(1 + (R1_{MIN}/R2_{MAX})) + (V_{REFMIN} - D_{LOW(MAX)} \bullet V_{OH(MIN)} + (1 - D_{LOW(MAX)}) \bullet V_{OL(MIN)})(R1_{MIN}/ (R3 + R4)_{MAX})$

17. $V_{OUTMIN(HIGH)} = V_{REFMAX}(1 + (R1_{MAX}/R2_{MIN})) + (V_{REFMAX} - D_{HIGH(MIN)} \bullet V_{OH(MAX)} + (1 - D_{HIGH(MIN)}) \bullet V_{OL(MAX)})(R1_{MAX}/ (R3 + R4)_{MIN})$

18. $V_{OUTMAX(HIGH)} = V_{REFMAX}(1 + (R1_{MAX}/R2_{MIN})) + (V_{REFMAX} - D_{LOW(MIN)} \bullet V_{OH(MAX)} + (1 - D_{LOW(MIN)}) \bullet V_{OL(MAX)})(R1_{MAX}/ (R3 + R4)_{MIN})$

19. $V_{OUTMIN(LOW)} = V_{REFMIN}(1 + (R1_{MIN}/R2_{MAX})) + (V_{REFMIN} - D_{HIGH(MAX)} \bullet V_{OH(MIN)} + (1 - D_{HIGH(MAX)}) \bullet V_{OL(MIN)})(R1_{MIN}/ (R3 + R4)_{MAX})$

Compensating for Errors in Digital Adjustment Circuitry

There are two common methods for overcoming the inaccuracies of the digital circuitry used to adjust the DC-DC converter (see Figures 4 and 5). Both involve measuring the output voltage of the DC-DC converter using an ADC, and using that measurement (or measurements) to compensate for the initial errors of the digital adjustment circuitry, and of the DC-DC converter.
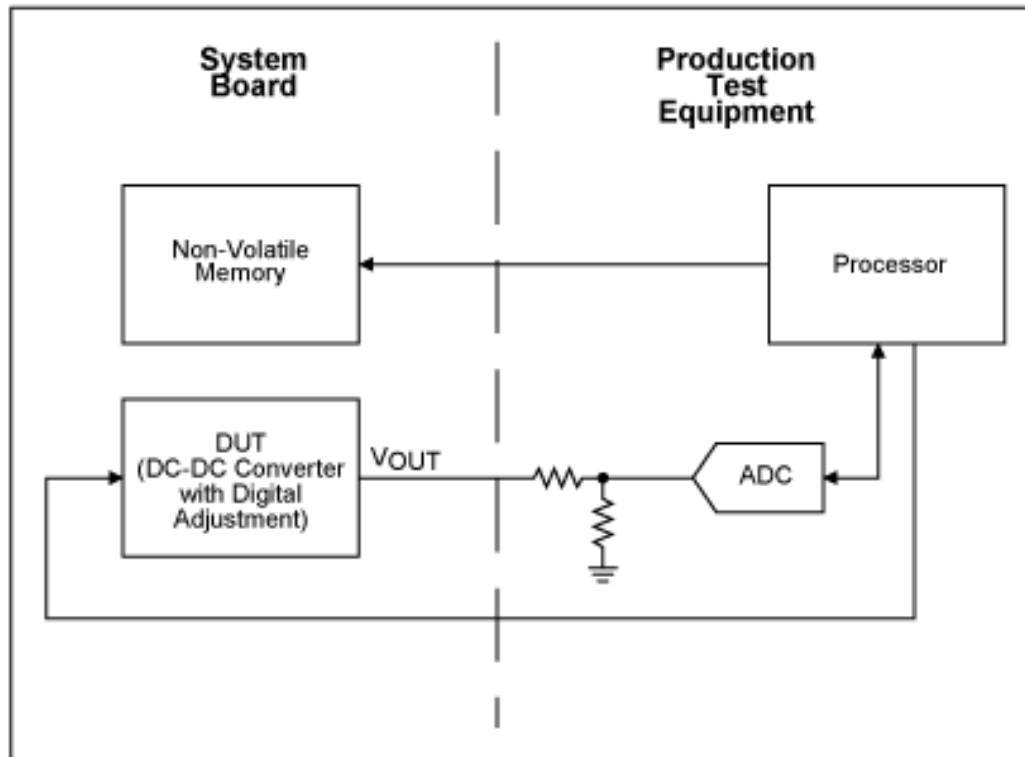

Figure 4. Measuring error of DC-DC converter and digital adjustment circuitry at production test.
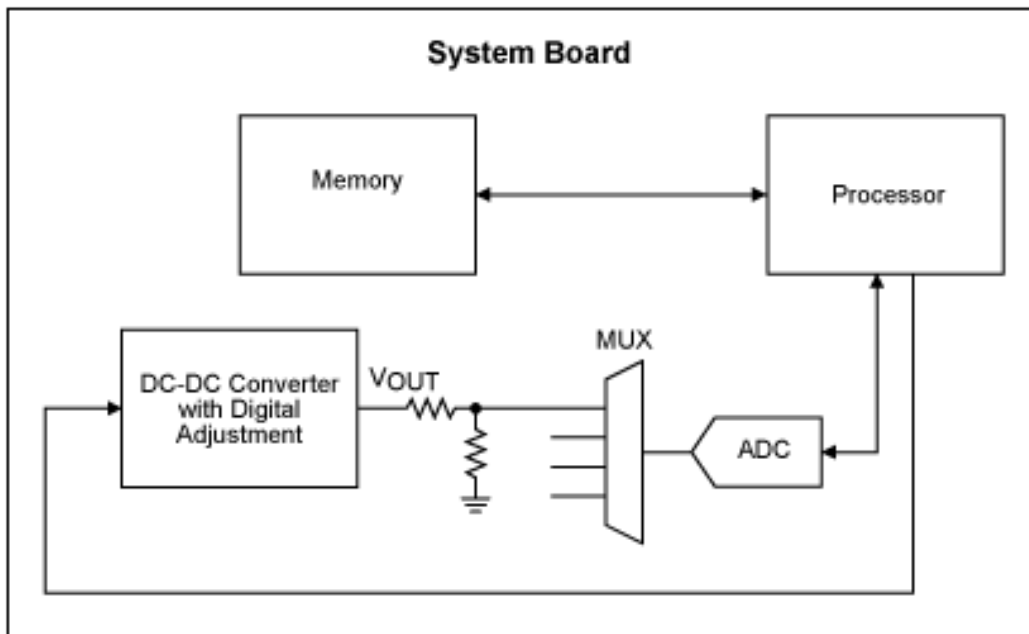
System Board

Memory ↔ Processor

DC-DC Converter with Digital Adjustment — VOUT — MUX — ADC

Figure 5. Measuring output of DC-DC converter and digital adjustment circuitry with on-board ADC.

One method uses the ADC on the system board (Figure 4), while the other uses the ADC on a piece of production test equipment (Figure 5). Each method has its own advantages and disadvantages.

The benefit of using the ADC on the system board is that it does not require a separate step at production test. Additionally, if the ADC is accurate over temperature, it can compensate for temperature drift errors inherent in the digital adjustment circuitry and in the DC-DC converter. Using the system ADC, however, requires that the on-board ADC be sufficiently accurate, and that it have a spare channel.

There are two common methods employed when using an ADC on the system board. The first entails measuring the DC-DC converter's output voltage every time the output code is changed. By monitoring the output voltage, one can avoid codes that would result in output voltages outside of the desired range.

The second method requires measurement of the DC-DC converter's output, typically when power is first applied to the device. The output voltage is measured with several different codes applied, allowing one to determine the initial errors such as offset and full-scale error (for an ADC), full-scale resistance (for a trim pot), or V_{OH} and V_{OL} (for a PWM signal). With knowledge of these initial errors, an algorithm can be used to avoid those codes that would result in output voltages outside the desired range.

When production test equipment is used to measure the errors of the adjustment circuitry and the DC-DC converter, the second compensation method (above) should be applied. A benefit of using production test equipment is that this method does not require a system ADC. Additionally, the measurement circuitry on the test equipment can be very expensive (and accurate, precise, etc.) without significantly increasing the cost of the end product, since its cost is spread out over the lifetime of the test equipment, whereas the cost of the system-board's ADC is built into each unit. And, if the devices are tested over temperature, temperature errors could also be eliminated. But testing over

temperature is typically too expensive, and is usually not needed

Overvoltage Issues

Many DACs power up to zero-scale, which causes V_{OUT} to be at its maximum value, as seen in the application circuit of Figure 1 (see equation 5). If $V_{OUTMAX(HIGH)}$ (Equation 8) exceeds the operating voltage range of the LCD supply, the DAC output must be raised to a value that does not allow the output of the DC-DC converter to get too high, before the DC-DC converter has powered up. One method of doing this is to keep the DC-DC converter powered off until the DAC output has been adjusted. Another method is to select a DAC that powers up to mid-scale, so that overvoltage issues are not a problem.

Similarly, for the PWM, make sure that its output is not set to zero with the LCD DC-DC converter powered-up; such a condition can cause VOUTMAX(HIGH) to exceed the limitations of the LCD device (see Figure 3 and Equation 18).

Many digital potentiometers power up to half-scale, which is a benign state for DC-DC converter adjustment. However, if powering up to half-scale causes $V_{OUTMAX(HIGH)}$ to exceed the limitations of the LCD device (see Figure 2 and Equation 13), then the DC-DC converter must be kept off until the potentiometer is set to a higher value.

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More Information

MAX5361: QuickView -- Full (PDF) Data Sheet -- Free Samples